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(54) Title: NOTCH-FREE ETCHING OF HIGH ASPECT SOI STRUCTURES USING ALTERNATING DEPOSITION AND ETCHING AND PULSED PLASMA

(57) Abstract: A method of preventing notching during a cyclical etching and deposition of a substrate with an inductively coupled plasma source is provided by the present invention. In accordance with the method, the inductively coupled plasma source is pulsed to prevent charge build up on the substrate. The off state of the inductively coupled plasma source is selected to be long enough that charge bleed off can occur, but not so long that reduced etch rates result due to a low duty cycle. The pulsing may be controlled such that it only occurs when the substrate is etched such that an insulating layer is exposed. A bias voltage may also be provided to the insulating layer and the bias voltage may be pulsed in phase or out of phase with the pulsing of the inductively coupled plasma source.

NOTCH-FREE ETCHING OF HIGH ASPECT SOI STRUCTURES USING ALTERNATING DEPOSITION AND ETCHING AND PULSED PLASMA

Cross References to Related Applications

This application claims priority from and is related to commonly owned U.S. Provisional Patent Application Serial No. 60/398,347 filed July 24, 2002, entitled: Notch-Free Etching of High Aspect SOI Structures Using Alternating Deposition and Etching and Pulsed ICP, this Provisional Patent Application incorporated by reference herein.

Field of the Invention

The present invention relates generally to the manufacture of silicon based micro-electro-mechanical-systems. More particularly, the present invention relates to the manufacture of high aspect ratio silicon structures using alternating deposition and etching steps with a pulsed inductively coupled plasma (ICP) source.

Background of the Invention

The fabrication of high aspect ratio features in silicon is used extensively in the manufacture of micro-electro-mechanical-systems (MEMS) devices. Such features frequently extend completely through the silicon wafer and may require etching in excess of 500μm into the silicon substrate. Even "shallow" features require etch depths up to 30μm with feature widths as small as 1μm, requiring the definition of structures with aspect ratios (depth/width) in excess of 30:1. To ensure economically feasible manufacturability, these processes must operate at high etch rates to maintain reasonable throughputs.

Conventional, single step, plasma etch processes cannot simultaneously meet these needs, and, thus alternative deposition/etching processes have been developed. For example, the process disclosed in U.S. Patents 4,985,114 and 5,501,893 use a high density plasma source, typically an Inductively Coupled Plasma (ICP), in conjunction with a radio frequency (RF) biased substrate electrode. Sulfur Hexafluoride (SF_6) is used as the etch gas and gases such as CCl_4 (4,985,114) or C_4F_8 (5,501,893) as the deposition gas. The process alternates with an interval of a few seconds between these two gases and results in silicon etch rates greater than 5μm/min with high aspect ratios and deep etches into silicon substrates. It should be noted that other high density plasma sources such as Electron Cyclotron Resonance (ECR) or Helicon can be used.

Certain MEMS devices require that the silicon substrate be etched down to a buried insulating layer, such as a silicon dioxide (SiO_2) layer, which acts as an etch stop. This structure is known as a Silicon On Insulator (SOI) structure which is required for functionality of the final device. When such structures are etched using a method such as disclosed in the '114 or '893 patent, "notching" occurs, which is a common reference to a well-documented phenomenon. Notching is evidenced as a severe undercutting of the silicon, localized at the silicon/insulator interface. It is generally understood that notching is caused by electrical charging effects during etching. Such effects are not present during the bulk etch because the silicon substrate is sufficiently conductive to ensure that current flow within the substrate prevents any charge separation. When the etch reaches the interface, the insulator is exposed and the conductive current path is broken, which allows charge separation to occur. Because of the different angular distributions of ions and electrons in the

plasma, ions (+ve charge) tend to accumulate at the bottom of the feature, and electrons (-ve charge) at the top. The resultant electric field is strong enough to bend the trajectories of arriving ions into the feature sidewall where lateral etching (notching) occurs. See KP Giapis, Fundamentals of Plasma Process-Induced Charging and Damage in *Handbook of Advanced Plasma Processing Techniques,* RJ Shul and SJ Pearton, Eds, Springer 2000.

The notching effect is more prevalent in high density plasmas, because the ion density, and therefore the charging effect due to the ions, is greater. The effect can be reduced by the use of a low density plasma, such as in conventional reactive ion etching (RIE), which is employed only after the insulator has been exposed. See Donohue et. al. U.S. Patent 6,071,822. The major drawback of such an approach is the low etch rate attainable, which is a serious shortcoming when features with various depths must be etched. This is a necessary consequence of etching devices with various feature sizes, which will etch to different depths due to Aspect Ratio Dependent Etching (ARDE).

The use of low frequency substrate bias in conjunction with an alternating deposition/etch process has been described as a solution to the notching phenomena, see Hopkins et. al. U.S. Patent 6,187,685. The same inventors also describe the use of a pulsed RF bias in conjunction with a high density etch process as an alternative means of reducing notching. Hopkins describes pulsing of the high density source (ICP) but concludes that this is ineffective in eliminating notching, and therefore teaches away from this approach as a possible solution.

U.S. Patents 5,983,828, 6,253,704 and 6,395,641 by Savas teach the use of a pulsed ICP to alleviate surface charging and subsequent notching. More specifically,

in the 5,983,828 Patent, Savas teaches pulsed ICP for eliminating notching, but limits the ICP operating powers to greater than 5kW. In the 6,253,704 and 6,395,641 Patents, Savas teaches pulsed ICP in conjunction with pulsed RF biased power. However, none of the pulsed ICP disclosures by Savas describe or suggest the use of pulsed ICP to eliminate notching for multi-step processes consisting of alternating deposition and etching steps.

Summary of the Invention

A preferred embodiment of the present invention is directed toward a method for anisotropically etching a substantially notch-free feature in a substrate. In accordance with this method, a substrate is subjected to an alternating cyclical process within a plasma chamber. The alternating cyclical process includes an etching step and a deposition step. An inductively coupled plasma source is pulsed during the etching step of the alternating cyclical process. Most preferably, the inductively coupled plasma source is pulsed when the substrate is etched and the insulating layer is exposed, and the inductively coupled plasma source is not pulsed when the substrate is etched and the insulating layer is not exposed. A bias voltage is provided to the substrate. The bias voltage may also be pulsed. The pulsing may be either in phase or out of phase with the pulsing of the inductively coupled plasma source. The bias voltage may be at an RF frequency or may be d.c.

Another embodiment of the present invention is directed toward a method of etching a feature in a silicon substrate provided on an insulating layer during a cyclical deposition/etch process. The method includes etching the substrate with an inductively coupled plasma from an inductively coupled plasma source while pulsing

the inductively coupled plasma source. The pulse width of an on state of the pulsed inductively coupled plasma source is selected such that charge build up does not reach a steady state. Typically, this condition is satisfied when a pulse width of an on state of the pulsed inductively coupled plasma source is less than a few milliseconds.

The above described embodiments of the present invention improve upon the prior art by reducing or eliminating notching at the junction of the substrate and the insulator. This is particularly beneficial when constructing high aspect ratio SOI structures where the notching that occurs may cause the structures to break loose from the substrate. Furthermore, the duration of the pulsing is selected such that the production time required to etch the substrate is not significantly increased. Therefore, the present invention represents a substantial improvement upon the prior art.

Brief Description of the Drawings

Fig. 1 is a depiction of a substrate and the notching that may occur during prior art methods of etching and deposition;

Fig. 2 is a depiction of the same feature as Fig. 1 etched using a pulsed inductively coupled plasma source in accordance with an embodiment of the present invention;

Fig. 3 is a depiction of a substrate etched in accordance with a preferred embodiment of the present invention; and

Fig. 4 is a flow chart of a method of etching a substrate in accordance with a preferred embodiment of the present invention.

Detailed Description of the Invention

Preferred embodiments of the present invention are directed toward a method and apparatus for reducing, or eliminating the notching observed when etching SOI structures. This is preferably accomplished by using an alternating deposition/etch process in conjunction with an ICP source which is pulsed between on and off states.

Referring to Fig. 1., a feature 2 etched in a substrate 4 that has been deposited on an insulating layer 8 without pulsing the ICP source is shown. The feature 2 is the result of etching an SOI structure using the process of the '893 patent with an approximate 2 minute over-etch (sufficient to etch other smaller structures). In such a process, notches 6 form at the junction of the substrate 4 and the insulating layer 8. The notch 6 at the silicon-insulator interface is evident, and extends ~ 3μm into the silicon. It can also be seen that the notches 6 undercut the feature 2 etched from the substrate 4. As the size of the feature to be constructed decreases, the undercutting caused by the notches 6 may severely damage the feature being constructed. More particularly, features with widths of ~ 4μm were undercut so badly that many were no longer attached to the substrate. Thus, in extreme cases, the notching 6 of the substrate 4 may result in the failure of the device being constructed from the substrate 4. It should be understood that other deposition/etch processes using a high density source (e.g., as described in the '114 patent) show similar effects.

To minimize or prevent the notching shown in Fig. 1, preferred embodiments of the present invention pulse the inductively coupled plasma source. The ICP source is preferentially pulsed during the etch cycle of the deposition/etch process, since this is when the notching primarily occurs. However, the ICP can also be pulsed through both deposition and etch cycles. The pulse width of the ICP on state should be short

enough that the charge build up does not reach a steady state, or is at a steady state for only a short period of time, and is of the order of a few microseconds to a few milliseconds. The ICP off state should be long enough that charge bleed off can occur, but not so long that reduced etch rates due to a low duty cycle result. The off time should also be of the order of a few microseconds to a few milliseconds. The pulse duty cycle should be in the range of 5-50%.

When the structure shown in Fig. 1 is etched using identical process conditions, except that the ICP is pulsed during the etch cycle (200μs on, 200μs off, 50% duty cycle) then the undercut at the silicon-insulator interface is dramatically reduced. This is shown in the cross section depicted in Fig. 2. The feature 10 etched in the substrate 4 of Fig. 2 using a pulsed ICP source has vastly reduced notches in the area of the junction between the substrate 4 and the insulating layer 8. This reduction in notching also dramatically reduces the risk that a narrow or deep feature will be undercut to an extent that the device being constructed will fail. The method used to produce the feature 10 of Fig. 2 can be implemented as a single step or multi-step process. In the single step implementation, pulsed ICP is used during the whole process. In the multi step implementation, the first step can be any suitable process resulting in the required etch profile and etch rate, but which is terminated before the underlying insulator is exposed. The ICP need only be pulsed for the period when the insulator film is exposed, since this is when the maximum benefit from charge reduction and notch reduction is expected. The etch is completed using a pulsed ICP "finish" etch to avoid notching at the silicon/insulator interface.

In accordance with an especially preferred embodiment, a substrate bias can be maintained "on" continuously during the etch cycle, or it to can be pulsed. This

pulsing of the bias voltage can be either in phase with the ICP pulse (i.e., the bias voltage is pulsed on when the ICP is on) or can be out of phase with the ICP (i.e., the bias voltage is pulsed on when the ICP is off). In the latter mode, use is made of the ion-ion plasma that exists briefly after the ICP power has been turned off. The substrate bias pulsing can be at a preferred frequency of 13.56 MHz or it can be at higher frequencies (e.g., 27, 40, 60 or 100MHz) or at lower frequencies (e.g., 50-500 kHz) or it can be d.c.

Fig. 3 depicts the results obtained by pulsing the ICP in connection with the construction of narrow or deep features 20. The narrow features 20 have widths of ~ 3μm surrounded by relatively large etched areas 24. The narrow features 20 have been etched with little or no undercut in the previously notched areas 26 at the substrate and insulator 22 junction.

Referring now to Fig. 4, a cyclical method of constructing a feature on a substrate in accordance with an embodiment of the present invention is shown. The method commences in block 30 with the performing of a deposition process on the substrate. The method then proceeds to block 34 wherein an etching process is performed on the substrate. While the etching step 34 is being performed, an ICP source used during the etching is pulsed 36. As discussed above, pulsing the ICP source minimizes or eliminates notching that occurs at the silicon-insulator junction. In addition, a substrate bias voltage is pulsed in block 32 during the etching step 34 to further reduce any notching. After the etching has been performed, the method proceeds to block 38 wherein the pulsing of the bias voltage and the inductively coupled plasma source is stopped. The method then returns to block 30 wherein

another deposition process is performed. The process is then repeated until the etching and deposition is finished.

It will be understood that the specific embodiments of the invention shown and described herein are exemplary only. Numerous variations, changes, substitutions and equivalents will now occur to those skilled in the art without departing from the spirit and scope of the present invention. Accordingly, it is intended that all subject matter described herein and shown in the accompanying drawings be regarded as illustrative only and not in a limiting sense and that the scope of the invention be solely determined by the appended claims.

What is claimed is:

1. A method for anisotropically etching a feature in a substrate comprising the steps of:

subjecting the substrate to an alternating cyclical process within a plasma chamber, said alternating cyclical process having an etching step and a deposition step; and

pulsing an inductively coupled plasma source during the etching step of the alternating cyclical process.

2. The method of claim 1 further comprising the step of providing a bias voltage to the substrate.

3. The method of claim 2 further comprising the step of pulsing the bias voltage.

4. A method of etching a feature in a silicon substrate provided on an insulating layer as part of a cyclical deposition/etching process, said method comprising etching the substrate with an inductively coupled plasma from an inductively coupled plasma source while pulsing the inductively coupled plasma source.

5. The method of claim 4 further comprising the step of providing a bias voltage to the substrate.

6. The method of claim 5 further comprising the step of pulsing the bias voltage provided to the substrate.

7. The method of claim 6 wherein the bias voltage is pulsed in phase with the pulsing of the inductively coupled plasma source.

8. The method of claim 6 wherein the bias voltage is pulsed out of phase with the pulsing of the inductively coupled plasma source.

9. The method of claim 6 wherein the bias voltage is at an RF frequency.

10. The method of claim 6 wherein the bias voltage is pulsed d.c.

11. The method of claim 4 wherein the step of etching the substrate further comprises only pulsing the inductively coupled plasma source when the insulating layer is exposed.

12. The method of claim 4 wherein a pulse width of an on state of the pulsed inductively coupled plasma source is selected such that charge build up does not reach a steady state.

13. The method of claim 4 wherein a pulse width of an on state of the pulsed inductively coupled plasma source is less than a few milliseconds.

14. A method of constructing a structure on a substrate, said method comprising alternatively performing a deposition step and an etching step wherein an inductively coupled plasma source is pulsed during the etching step to prevent notching.

15. The method of claim 14 further comprising the step of providing a bias voltage to the substrate.

16. The method of claim 14 further comprising pulsing the bias voltage.

17. The method of claim 16 wherein the bias voltage is pulsed in phase with the pulsing of the inductively coupled plasma source.

18. The method of claim 16 wherein the bias voltage is pulsed out of phase with the pulsing of the inductively coupled plasma source.

19. The method of claim 15 wherein the step of pulsing the inductively coupled plasma source further comprises pulsing the inductively coupled plasma source when the etching step exposes an insulating layer.

20. The method of claim 15 wherein a pulse width of an on state of the pulsed inductively coupled plasma source is selected such that charge build up on the substrate does not reach a steady state.

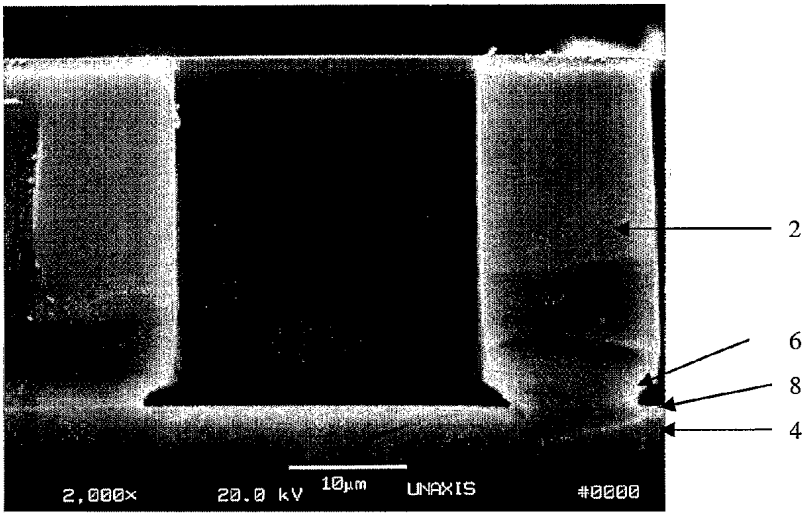

Figure 1 SOI feature etched using no pulsing (prior art)

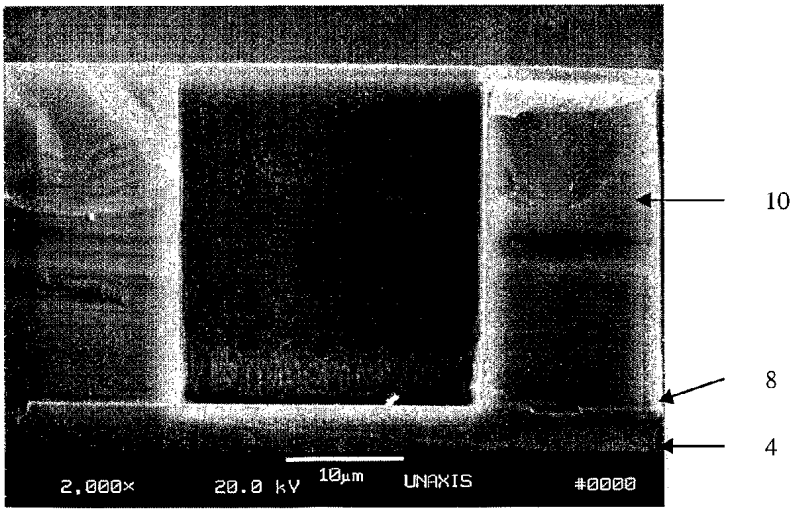

Figure 2 Same feature as Fig 1, using ICP pulsing

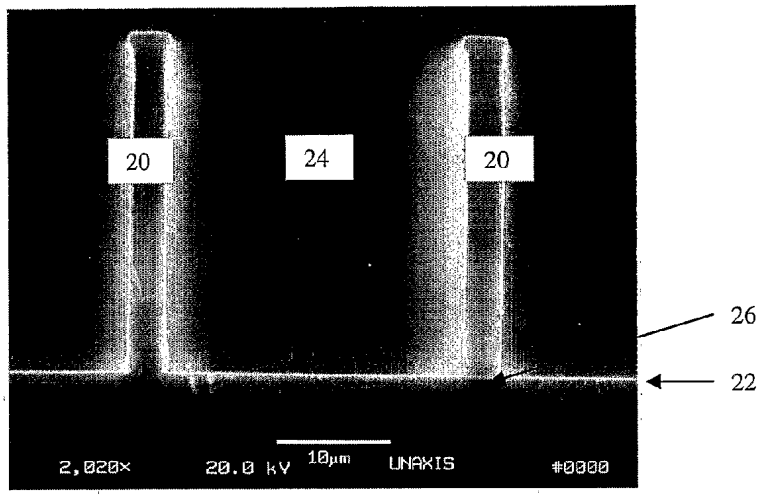

Figure 3 Narrow features etched in an SOI structure using ICP pulsing

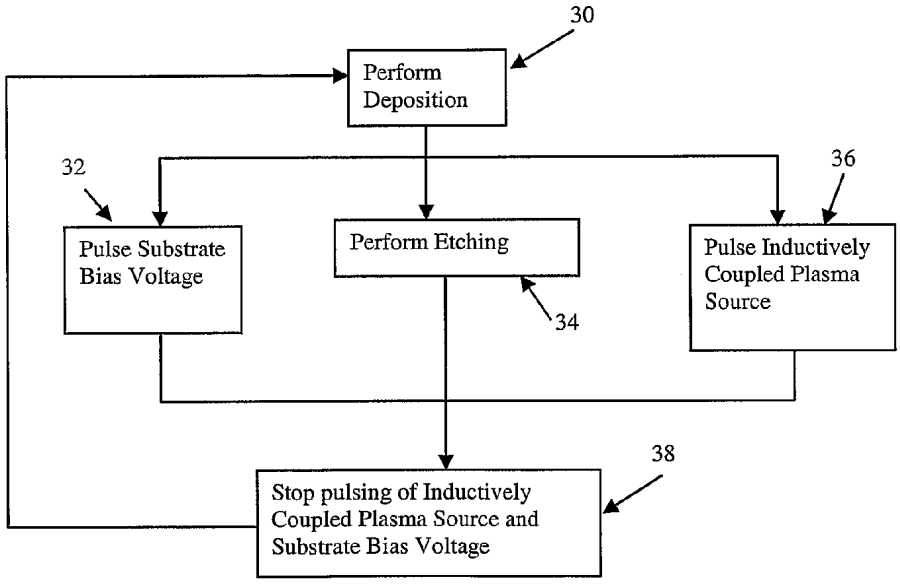

Fig. 4